

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In restatent Application of

Abdalla Aly Naem, et al.

Application No. 10/772,863

Filed: February 4, 2004

For: METHOD OF FORMING A MOS

TRANSISTOR WITH A LAYER OF SILICON GERMANIUM CARBON (as

amended)

Group Art Unit: 2823

Examiner: William M. Brewster

INFORMATION DISCLOSURE

STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Applicants submit herewith information of which applicants are aware, which applicants believe may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

This Information Disclosure Statement:

- (a) [X] accompanies a RCE transmittal submitted herewith. 37 CFR § 1.97(a).
- (b) [] is filed within three months after the filing date of the application or within three months after the date of entry of the national stage of a PCT application as set forth in 37 CFR § 1.491.
- (c) [] as far as is known to the undersigned, is filed before the mailing date of a first Office Action on the merits.

(d) []	is filed after the first office action and more than three months after the
	application's filing date or PCT national stage date of entry filing but, as far
	as is known to the undersigned, prior to the mailing date of either a final
	rejection or a notice of allowance, whichever occurs first, and is accompanied
	by either the fee (\$180) set forth in 37 CFR § 1.17(p) or a certification as
	specified in 37 CFR § 1.97(e), as checked below.

(e) [] is filed after the mailing date of either a final rejection or a notice of allowance, whichever occurred first, and is accompanied by the fee (\$180) set forth in 37 CFR § 1.17(i)(1) and a certification as specified in 37 CFR § 1.97(e), as checked below. This document is to be considered as a petition requesting consideration of the information disclosure statement.

[If either of boxes (d) or (e) are checked above, the following "certification" under 37 CFR § 1.97(e) may need to be completed.] The undersigned certifies that:

- (f) [] Each item of information contained in the information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.
- (g) [] No item of information contained in this information disclosure statement was cited in a communication mailed from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of this information disclosure statement.

A list of the patent(s) or publications(s) is set forth on the attached Form PTO-1449 (Modified). A copy of the items on PTO-1449 (Modified) is supplied herewith:

- (h) [] each
- (i) [] none
- (j) [X] only those listed below:

Stanley Wolf et al., "Silicon Processing For The VLSI Era", Volume 1, Process Technology, Lattice Press, 1986, pp. 155.

Those patent(s) or publication(s) which are marked with an asterisk (*) in the attached form PTO-1449 (Modified) are not supplied because they:

- [] were previously cited by or submitted to the Office in a prior application no. ______ filed _____ and relied upon in this application for an earlier filing date under 35 U.S.C. § 120 or
- [X] are hereby waived pursuant to 37 CFR 1.98 (a)(2)(i) for all U.S. national patent applications filed after June 30, 2003.

A concise explanation of relevance of the described above and attached information

(k) [X] not given

is:

(1)	[]	given for each listed item						
(m)	[]	given for only non-English language listed item(s) [Required]						
(n)	[]	is in the form of an English language copy of a Search Report from a foreign patent office, issued in a counterpart application, which refers to the relevant portions of the references [copy attached].						

While the information disclosed in this Information Disclosure Statement may be "material" pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that the information referred to is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR § 1.56(a) exists. It is submitted that the Information Disclosure Statement is in compliance with 37 CFR § 1.98 and MPEP § 609 and the Examiner is respectfully requested to consider the above-described and attached information.

Respectfully submitted,

Dated: 4-19-00

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Attorney for Assignee

Atty. Docket No: 100-19811 (P05402-D01-F2)

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APR 1	9 200	S	U	.s. patent	DOCUMENTS	<u> </u>				
EXAMINER INITIAL		DOCUMENT NUMBER	DATE		NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE		
7774	DENA	*6,103,603	08/15/00	Han		438	532	04/24/98		
		*6,512,252 B1	01/28/03	Takagi,	et al.	257	192	11/15/00		
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			U.S. PATER	NT APPLICA	ATION PUBLICATIONS	s				
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	CUMENT NUMBER DATE		NAME CLASS		SUBCLASS	1	FILING DATE IF APPROPRIATE	
		*2002/0179946 A1	12/05/02	Hara, e	t al.	257	288	04/18/01		
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			OTHER	DOCUMEN	TTS (Including A	uthor, Title, Date, Pe	ertinent Pages, E	tc.)		
		Stanley Wolf, et al., "	Silicon Processing	; For The V	LSI Era", Volume 1,	Processing Techno	ology, Lattice l	Press, 1986,	, pp. 155.	
EXAMINER					DATE CONSIDERED					
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Form PTO-A820 (also form PTO-1449)

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